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(71) Applicant: **NEC CORPORATION**
7-1, Shiba 5-chome Minato-ku
Tokyo 108-01(JP)

(72) Inventor: **Toeda, Masahiro**
c/o NEC Corporation, 7-1, Shiba 5-chome
Minato-ku, Tokyo(JP)

(74) Representative: **Glawe, Delfs, Moll & Partner**
Patentanwälte
Postfach 26 01 62
W-8000 München 26(DE)

(54) **Intrinsic gettering for a semiconducteur epitaxial wafer.**

(57) An epitaxial wafer is manufactured through a process for forming a silicon epitaxial layer on a silicon substrate having an oxygen concentration of 16 to 19 x $10^{17}/cm^3$ and a heat treatment of the system at 650 °C ~ 900 °C for one hour ~ five hours.

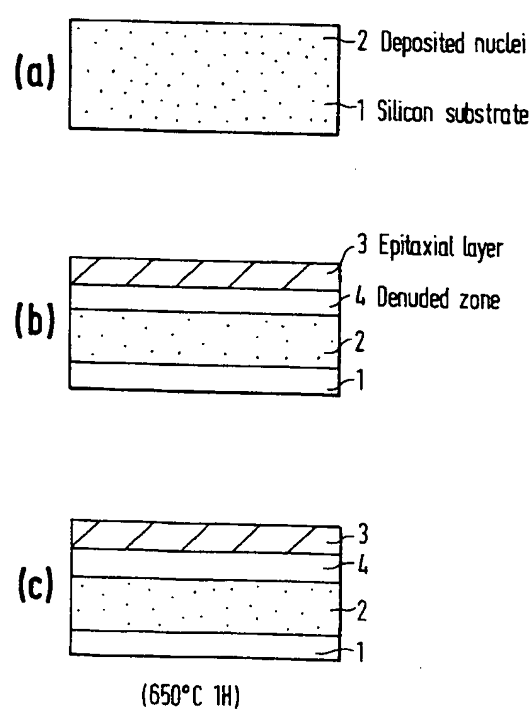

FIG.1

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BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a manufacturing method of a semiconductor epitaxial wafer, and more particularly, to a manufacturing method of an epitaxial wafer which is given an intrinsic gettering effect.

Description of the Related Art

The process for getting rid of impurities or defects, like alkali metals such as Na, heavy metals such as Fe, or crystal defects, that are harmful to semiconductor devices is generally called gettering. In particular, the process for creating segregation spots by utilizing super-saturated oxygens that are intrinsic to an Si wafer is called intrinsic gettering.

According to the intrinsic gettering, first, oxygens in the surface part are diffused out by subjecting a Si wafer containing super-saturated oxygens to a heat treatment, then oxygens in the interior of the wafer are derived out. As a result, a denuded zone which has neither oxygen deposition nor crystal defect is formed in the surface part that constitutes the device, while a sink for impurities and defects that have oxygen deposition and crystal defect at high density is formed in the interior of the wafer.

In the method of manufacturing a semiconductor device using the intrinsic gettering process first a silicon substrate with oxygen concentration of 12 to 15 x $10^{17}/cm^3$ is prepared. The minute deposited nuclei that exist in the silicon substrate are removed by heat treatments first at a high temperature of 1150°C for about 3 hours, then at 650°C for about 24 hours to obtain a denuded zone free from deposited nuclei in the top and the bottom surfaces of the silicon substrate. Following that, an epitaxial layer is formed on the surface of the substrate.

Since resistivity of the substrate is set to be 0 to 0.018 Ω•cm and the resistivity of the epitaxial layer is set to be on the order of 15 Ω•cm in the prior art epitaxial wafer, it becomes necessary to raise the concentration of the impurity (for example, Sb) in the silicon substrate. As a result, the oxygen concentration in the silicon substrate to be used was in the range of 12 to 15 x $10^{17}/cm^3$ for the reason of the relation between the concentration partial pressures.

In the conventional method of manufacturing an epitaxial wafer, silicon is epitaxially grown after heat treatments at a high and at a low temperatures of the silicon substrate having an oxygen concentration of 12 to 15 x $10^{17}/cm^3$. Since there exist irregularities in the oxygen concentration of the silicon substrate, some uncertainity of the treatment time cannot be avoided. Thus, it is necessary to select an appropriate time for respective substrates so as to permit an adequate outward diffusion of oxygens, in the high temperature (for example, 1150°C) heat treatment. Moreover, a long heat treatment of about 24 hours was required for the low temperature (for example, 650°C) heat treatment because of the low oxygen concentration of 12 to 15 x $10^{17}/cm^3$ of the silicon substrate. For these reasons, there was a problem that the productivity is poor and the cost becomes high for the epitaxial wafers.

SUMMARY OF THE INVENTION

It is an object of the invention to enhance the productivity and reduce the cost of the epitaxial wafer, and to carry cut an intrinsic gettering processing after growing an epitaxial layer on a silicon substrate.

According to the present invention, an epitaxial layer is grown on a semiconductor substrate having an oxygen concentration of 16 ~ 19 x 10^{17} cm^{-3} at a temperature above 1000°C, then subjected to an intrinsic gettering process. Thus, the heat treatment for intrinsic gettering needs to be carried out at low temperature of 650°C for only 1 hour, cutting down markedly the time for the heat treatment.

BRIEF DESCRIPTION OF THE DRAWING

FIG. 1(a) ~ FIG. 1(c) shows the sectional views illustrating a preferred embodiment of the manufacturing method of an epitaxial wafer according to the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

As shown in FIG. 1(a), an Sb-containing N-type silicon substrate 1 having an oxygen concentration of 16 to 19 x $10^{17}/cm^3$ is prepared. This silicon substrate 1 includes minute deposited nuclei 2. Next, as shown in FIG. 1(b), an epitaxial layer 3 with thickness of about 15 µm is formed at 1150°C on the surface of the silicon substrate 1 by means of a chemical vapor deposition (CVD) method using, for example, $SiHC\ell_3$-H_2 gas. The temperature for this process suffices if it is 900 ~ 1200°C. This epitaxial growth process correspondes, in function, to the high temperature heat treatment at 1150°C in the prior art method. During this epitaxial growth process, there is formed a denuded zone 4 in the silicon substrate 1. Next, as shown in FIG. 1(c), deposited nuclei 2 are grown by a heat treatment at a low temperature of 650°C for 1 hour. This

heat treatment is generally enough to heat at 650°C ~ 900°C for 1 hour ~ 5 hours in an atmosphere of nitrogen, oxygen, vapor and so on.

According to this embodiment, use is made as the silicon substrate 1 a substrate with oxygen concentration raised to a high level which facilitates the formation of the deposited nuclei, so that it is possible to cut down the time for heat treatment at the low temperature from the conventional value of about 24 hours to about 1 ~ 5 hours. Following the low temperature heat treatment, during the element manufacturing process, gettering of contaminating impurities and microdefects are continued to be carried out in the following heat treatments of the impurity-diffusion process, etc. From what has been described in the above, it can be seen that an enhancement of the productivity and a reduction of the manufacturing cost can be realized as a result of a sharp curtailment of the heat treatment time and a reduction of the process number. It should be noted that when the heat treatment time and the temperature of the element manufacturing process differ markedly from those of the aforementioned example, appropriate control, such as selection of the time for the low temperature heat treatment, may be needed to obtain sufficient intrinsic gettering effect.

It is to be further noted that the reason for setting the upper limit of the oxygen concentration of the silicon substrate at 19 x $10^{17}/cm^3$ is that there will be generated surface defects in the epitaxial layer for oxygen concentration above that value.

As described in the above, this invention makes it possible to cut down the high temperature heat treatment which was required in the prior art and to reduce sharply the time of heat treatment at low temperature, by forming an epitaxial layer on the silicon substate whose oxygen concentration is raised to 16 to 19 x $10^{17}/cm^3$, then giving a heat treatment at low temperature. Therefore, this invention has an effect of enabling to enhance the productivity and to reduce the cost of the epitaxial wafers.

Claims

1. A method for manufacturing a semiconductor wafer comprising steps of: forming a semiconductor layer on a semiconductor substrate having an oxygen concentration of 16 to 19 x $10^{17}/cm^3$, and subjecting to an intrinsic gettering process.

2. A method for manufacturing a semiconductor wafer according to claim 1, wherein said semiconductor wafer is a silicon wafer and a silicon epitaxial layer is grown on said silicon wafer as said semiconductor layer, thereafter subjecting the system to said intrinsic gettering.

3. A method for manufacturing a semiconductor wafer according to claim 2, wherein said intrinsic getting comprises a heating step at 650°C ~ 900°C for 1 hour ~ 5 hour.

4. A method for manufacturing an epitaxial wafer comprising steps of: growing a silicon epitaxial layer at a temperature higher than 1000°C on a silicon substrate having an oxygen concentration of 16 to 19 x $10^{17}/cm^3$, subjecting the system having said epitaxial layer on said substrate to an intrinsic gettering process.

5. A method for manufacturing an epitaxial wafer according to claim 4, wherein said silicon epitaxial layer is grown at 1000°C ~ 1200°C, and said intrinsic gettering process is carried out at 600°C ~ 900°C for 1 hour ~ 5 hours.

6. A method for manufacturing a silicon epitaxial wafer comprises steps of, growing a silicon epitaxial layer at a temperature of 900°C ~ 1200°C on a silicon substrate having an oxygen concentration of 16 to 19 x $10^{17}/cm^3$, subjecting the system to a heat treatment at 650°C ~ 900°C for 1 ~ 5 hours.

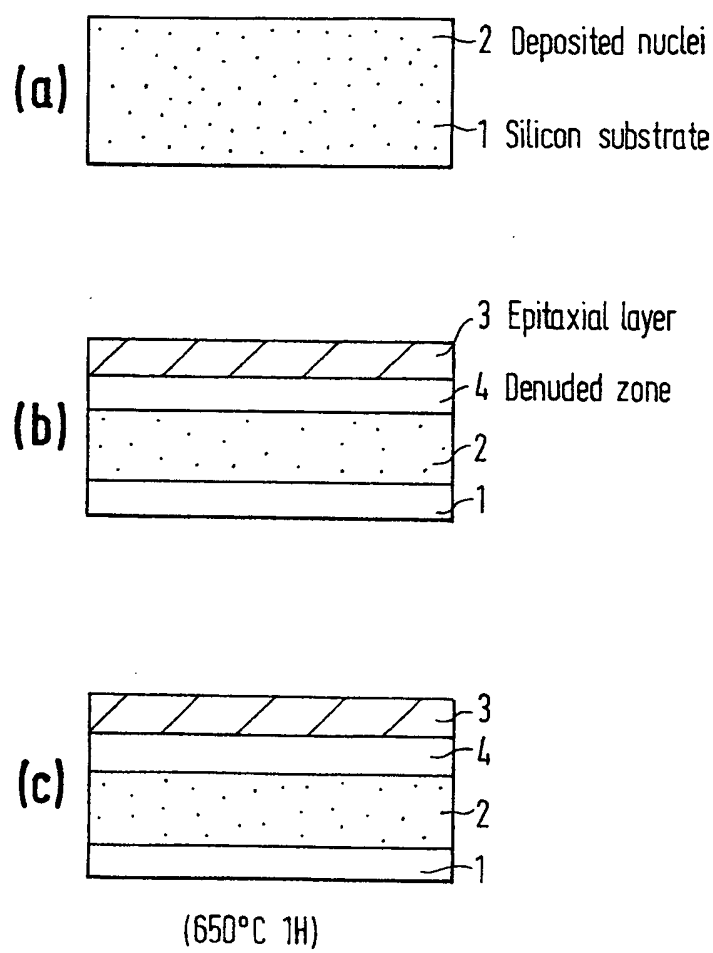
(a)
2 Deposited nuclei
1 Silicon substrate
(b)
3 Epitaxial layer
4 Denuded zone
2
1
(c)
3
4
2
1
(650°C 1H)

FIG.1

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(71) Applicant: **NEC CORPORATION**
7-1, Shiba 5-chome Minato-ku
Tokyo 108-01(JP)

(72) Inventor: **Toeda, Masahiro**
c/o NEC Corporation, 7-1, Shiba 5-chome
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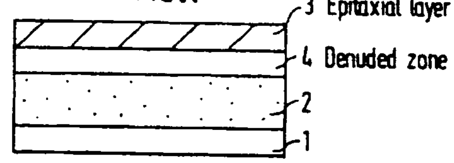
FIG.1

(b)



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EUROPEAN SEARCH REPORT

Application Number

EP 92 10 1022

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
X	PATENT ABSTRACTS OF JAPAN vol. 12, no. 342 (E-658)14 September 1988 & JP-A-63 104 322 (TOSHIBA CORP) 9 May 1988 * abstract *	1,2	H01L21/322 H01L21/205
A		4,6	
A	PATENT ABSTRACTS OF JAPAN vol. 10, no. 42 (E-382)19 February 1986 & JP-A-60 198 832 (NIPPON DENKI) 8 October 1985 * abstract *	1,4,6	
A	PATENT ABSTRACTS OF JAPAN vol. 12, no. 481 (E-694)15 December 1988 & JP-A-63 198 334 (KOMATSU DENSHI KINZOKU) 17 August 1988 * abstract *	1-6	
A	GB-A-2 080 780 (THE SECRETARY OF STATE FOR DEFENSE) * column 1, line 85 - line 106 *	1,4,6	TECHNICAL FIELDS SEARCHED (Int. Cl.5)
			H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
BERLIN	05 MAY 1993	LE MINH I.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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A : technological background
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E : earlier patent document, but published on, or after the filing date
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